AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A method of reducing power consumption in a semiconductor memory device having a row of memory cells and circuitry for operating the row of memory cells, the method comprising the steps of:

providing an intervention circuit;

instantiating the intervention circuit within the circuitry for operating the row of memory cells, proximal to the row of memory cells;

operating the intervention circuit to retain the row of memory cells in a desired state; and

powering down, with a power switch, the circuitry for operating the row of memory cells preceding the intervention circuit;

wherein the intervention circuit is operated by a first signal source, separate from a second signal source that powers down the circuitry for operating the row of memory cells preceding the intervention circuit.

2. (Original) The method of claim 1, wherein the row of memory cells comprises a wordline and the circuitry for operating the row of memory cells comprises driver circuitry.

3. (Original) The method of claim 1, wherein the intervention circuit comprises a resistor.

4. (Original) The method of claim 1, wherein the intervention circuit comprises a transistor.

5. (Previously Presented) The method of claim 2, wherein the intervention circuit is instantiated such that a driver transistor pair of the driver circuitry is between the intervention circuit and the wordline.

6. (Original) The method of claim 2, wherein the intervention circuit is instantiated between the wordline and driver circuitry.

7. (Previously Presented) The method of claim 1, wherein the steps of operating the intervention circuit and powering down the circuitry for operating the row of memory cells preceding the intervention circuit are not performed concurrently.

8. (Cancelled)

9. (Previously Presented) The method of claim 1, wherein a nominal delay follows the step of operating the intervention circuit before powering down the circuitry for operating the row of memory cells preceding the intervention circuit is performed.

10. (Cancelled)

11. (Currently Amended) A semiconductor device comprising:

a row of memory cells;

control circuitry preceding the row of memory cells; and

an intervention circuit, instantiated within the control circuitry proximal to the row of memory cells, adapted to hold the row of memory cells at a desired state while control circuitry preceding the intervention circuit is powered down with a power switch having a non-address control signal input, wherein the power switch is not located within the control circuitry.

12. (Original) The device of claim 11, wherein the row of memory cells comprises a wordline and the control circuitry preceding the row of memory cells comprises driver circuitry.

13. (Currently Amended) A semiconductor device comprising:

a row of memory cells;

control circuitry preceding the row of memory cells; and

an intervention circuit, instantiated within the control circuitry proximal to the row of memory cells, adapted to hold the row of memory cells at a desired state while control circuitry preceding the intervention circuit is powered down with a power switch having a control signal input, wherein the power switch is not located within the control circuitry ~~The device of claim 11~~, wherein the intervention circuit comprises a resistor.

14. (Original) The device of claim 11, wherein the intervention circuit comprises a transistor.

15. (Previously Presented) The device of claim 12, wherein the intervention circuit is instantiated such that a driver transistor pair of the driver circuitry is between the intervention circuit and the wordline.

16. (Original) The device of claim 12, wherein the intervention circuit is instantiated between the wordline and driver circuitry.

17. (Original) The device of claim 12, wherein the intervention circuit is coupled to a first assertion signal source that is also coupled to the driver circuitry.

18. (Currently Amended) A semiconductor device comprising:

a row of memory cells;

control circuitry preceding the row of memory cells; and

an intervention circuit, instantiated within the control circuitry proximal to the row of memory cells, adapted to hold the row of memory cells at a desired state while control circuitry preceding the intervention circuit is powered down with a power switch having a control signal input, wherein the power switch is not located within the control circuitry, wherein the row of memory cells comprises a wordline and the control circuitry preceding the row of memory cells comprises driver circuitry, and further ~~The device of claim 12~~, wherein the intervention circuit is coupled to a first assertion signal source, and a second assertion signal source is coupled to the driver circuitry.

19-22. (Cancelled)

23. (Previously Presented) The method of Claim 1, wherein the circuitry for operating the row of memory cells preceding the intervention circuit comprises a wordline pre-driver circuit.

24. (Previously Presented) The method of Claim 11, wherein the control circuitry preceding the intervention circuit comprises a wordline pre-driver circuit.

25. (Previously Presented) The method of Claim 11, wherein the control signal input is a sleep mode control signal.